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1. A semiconductor memory comprising a memory cell matrix including a plurality of cell columns arranged along a row-direction, each of cell columns is implemented by a plurality of memory cell transistors serially arranged along a column-direction, the memory cell matrix comprising:

a plurality device isolation films running along the column direction, arranged alternatively between the cell columns;

a plurality of first conductive layers arranged along the row and column-directions, a group of the first conductive layers arranged along one of column-direction is assigned to a corresponding cell column, adjacent groups of the first conductive layers are isolated from each other by the device isolation film disposed between the adjacent groups;

a plurality of lower inter-electrode dielectrics arranged respectively on crests of the corresponding first conductive layers, each of the lower inter-electrode dielectrics is made of insulating material containing at least silicon and nitrogen;

an upper inter-electrode dielectric arranged both on the device isolation films and the lower inter-electrode dielectric so that the upper inter-electrode dielectric can be shared by the memory cell transistors arranged along the row-direction belonging to different cell columns, the upper inter-electrode dielectric is made of insulating material different from the lower inter-electrode dielectrics; and

a plurality of second conductive layers running along the row-direction, each of the second conductive layers arranged on the upper inter-electrode dielectric so that the second conductive layer can be shared by the memory cell transistors arranged along the row-direction belonging to different cell columns.

2. The semiconductor memory of claim 1, further comprising a plurality of word lines running along the row-direction, each of the word lines is electrically connected to corresponding one of the second conductive layers.

3. The semiconductor memory of claim 2, further comprising a plurality of bit lines running along the column-direction, each of the word lines is shared by corresponding one of the cell columns.

4. The semiconductor memory of claim 3, further comprising:

a plurality of select transistors assigned respectively to end portions of corresponding cell columns; and

a select gate line electrically connected to gates of the select transistors.

5. The semiconductor memory of claim 1, wherein each of the lower inter-electrode dielectrics extends from the crest to the side surface of the first conductive layer so that a farthest end of the extending lower inter-electrode dielectric is sandwiched between the side surface of the first conductive layer and a side surface of corresponding device isolation film.

6. The semiconductor memory of claim 1, wherein each of the lower inter-electrode dielectrics is silicon

nitride film containing other elements than silicon and nitrogen less than approximately 20%.

7. The semiconductor memory of claim 1, wherein each of the upper inter-electrode dielectrics is a single layer film selected from the group consisting of an aluminum oxide film, a hafnium oxide film and a zirconium oxide film or a composite film including at least one of the single layer film.